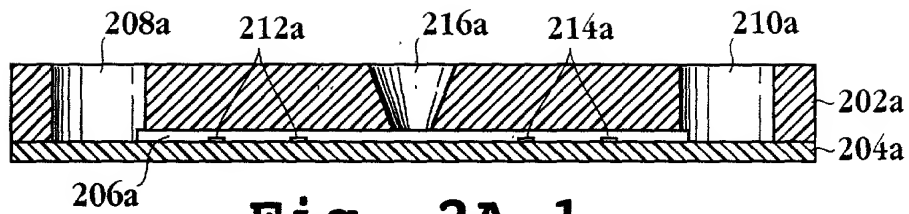
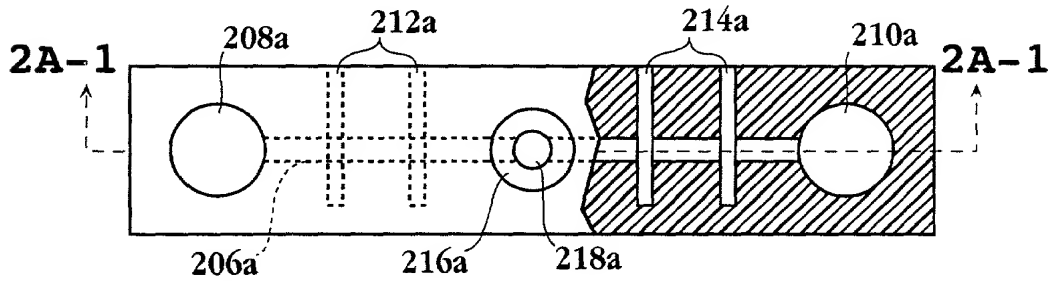


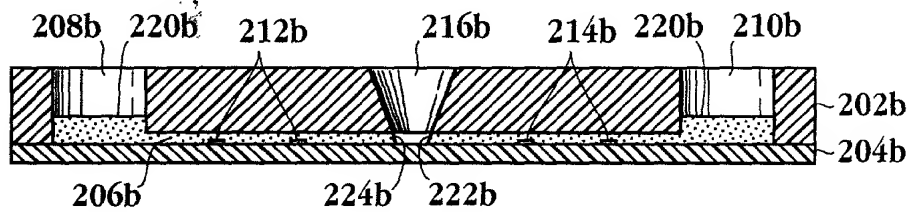
**Fig. 1**



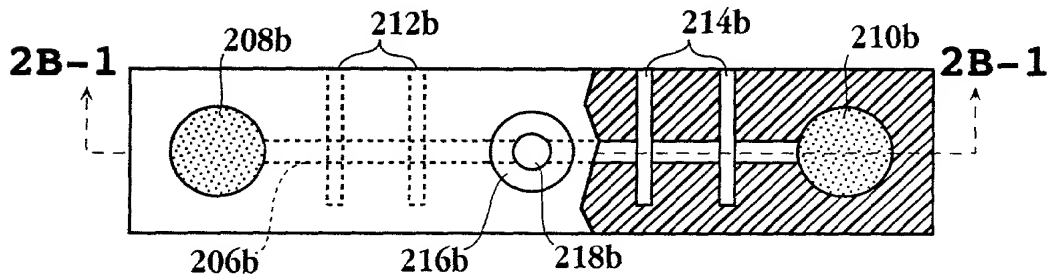
**Fig. 2A-1**



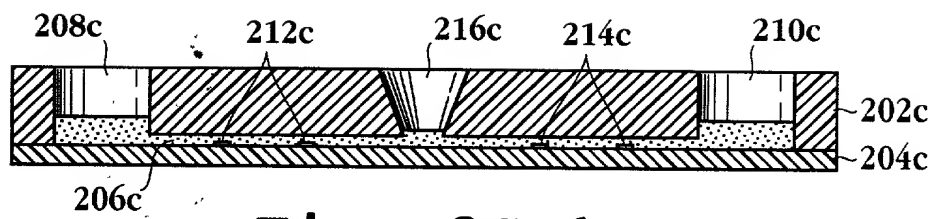
**Fig. 2A**



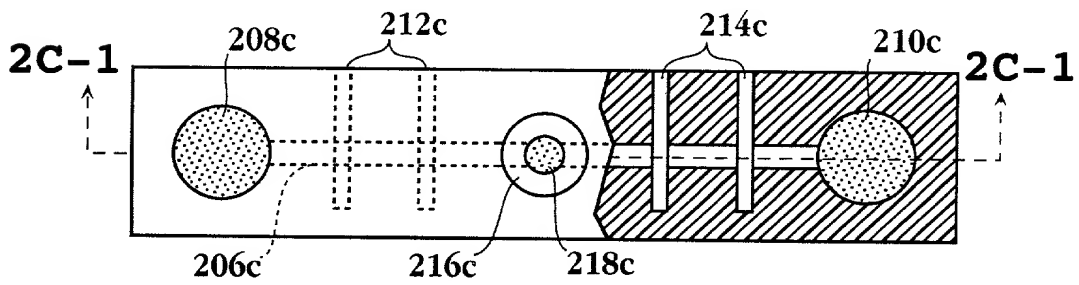
**Fig. 2B-1**



**Fig. 2B**

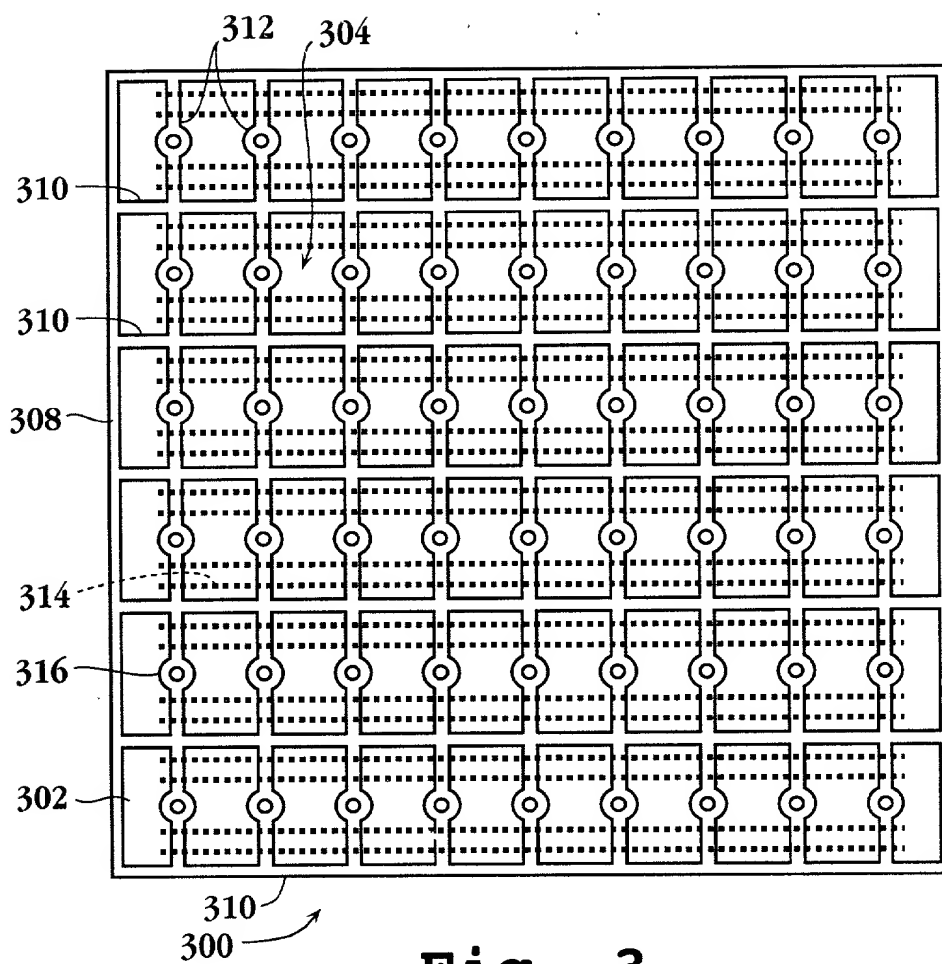


**Fig. 2C-1**



**Fig. 2C**

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**Fig. 3**

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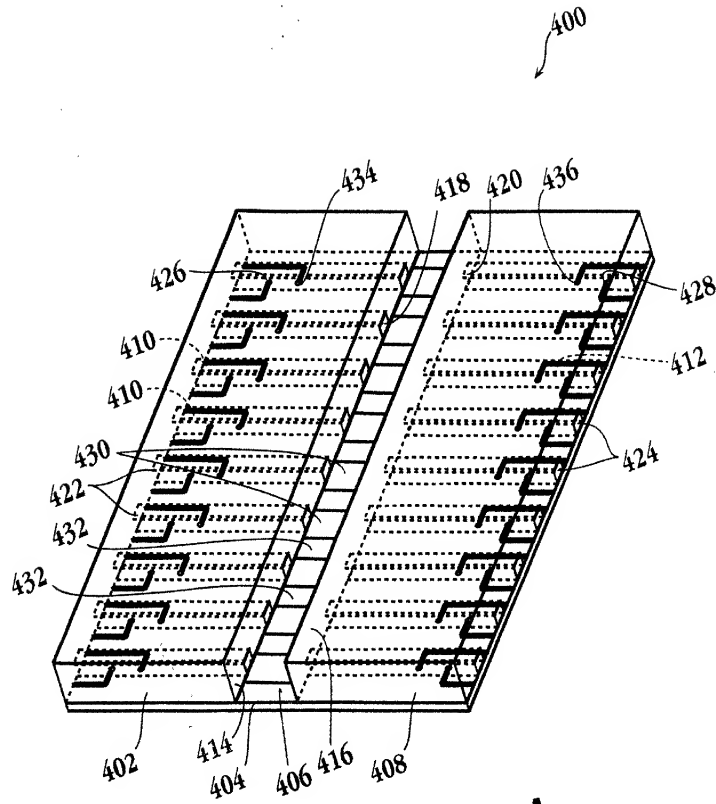
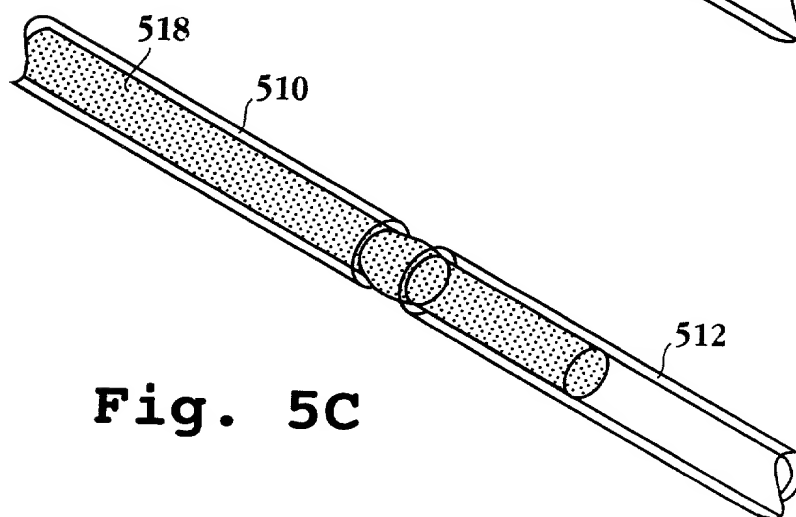
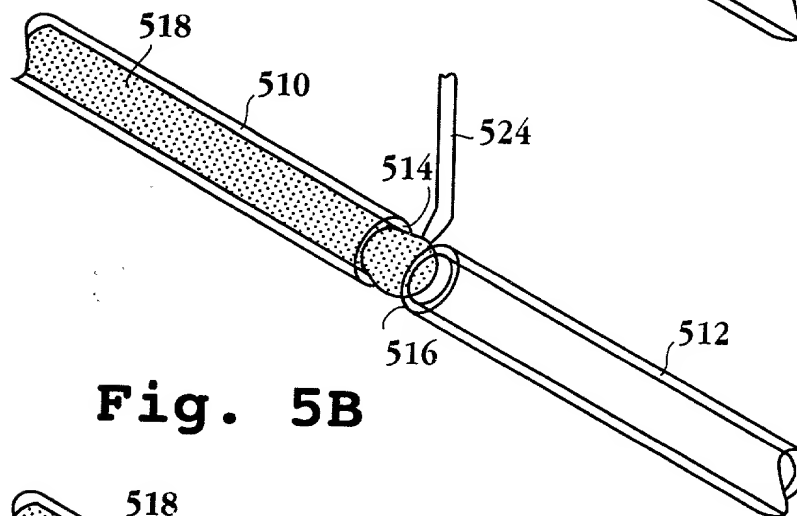
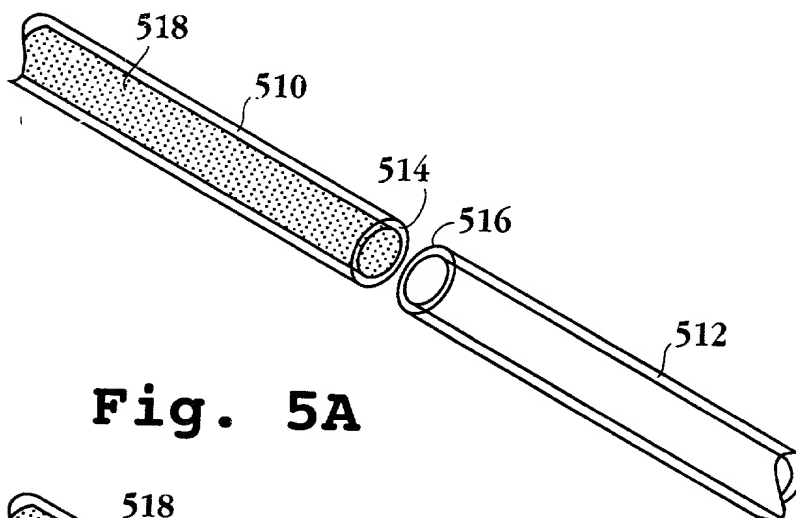
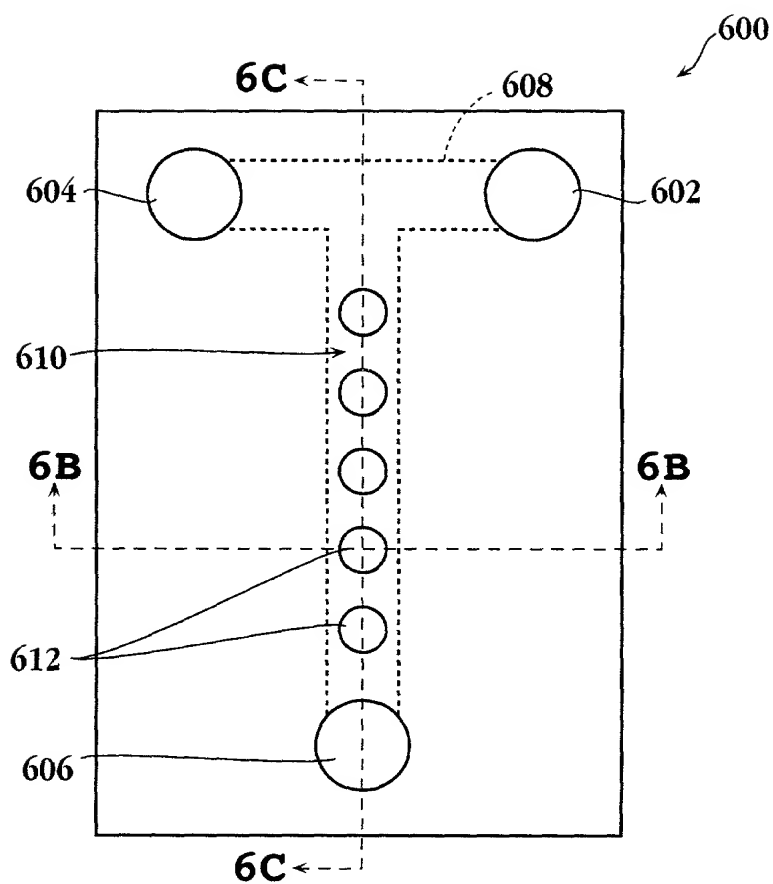


Fig. 4

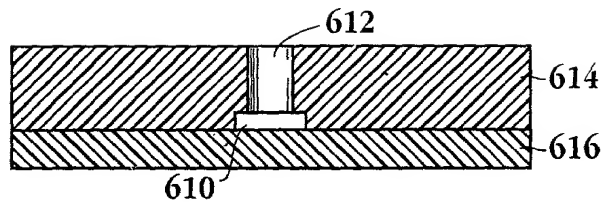
2006-01-01 09:59:56



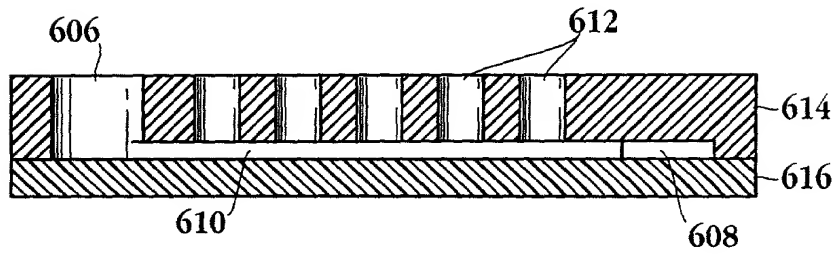
2025 RELEASE UNDER E.O. 14176



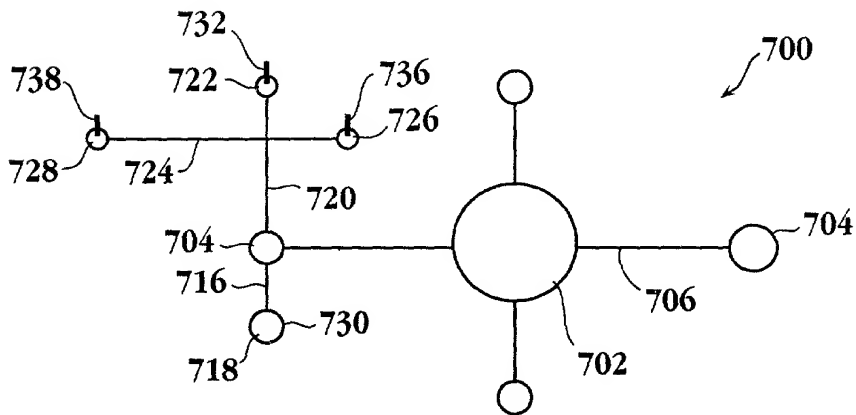
**Fig. 6A**



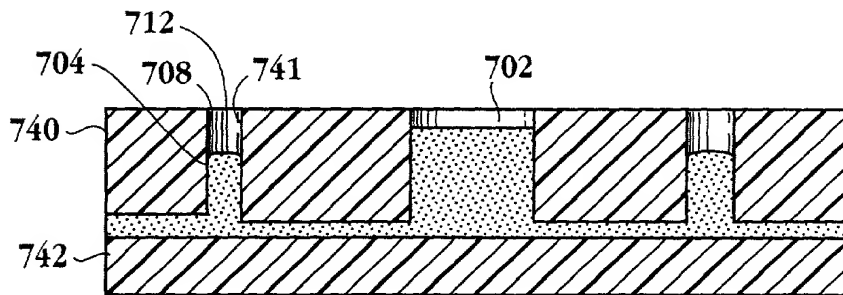
**Fig. 6B**



**Fig. 6C**



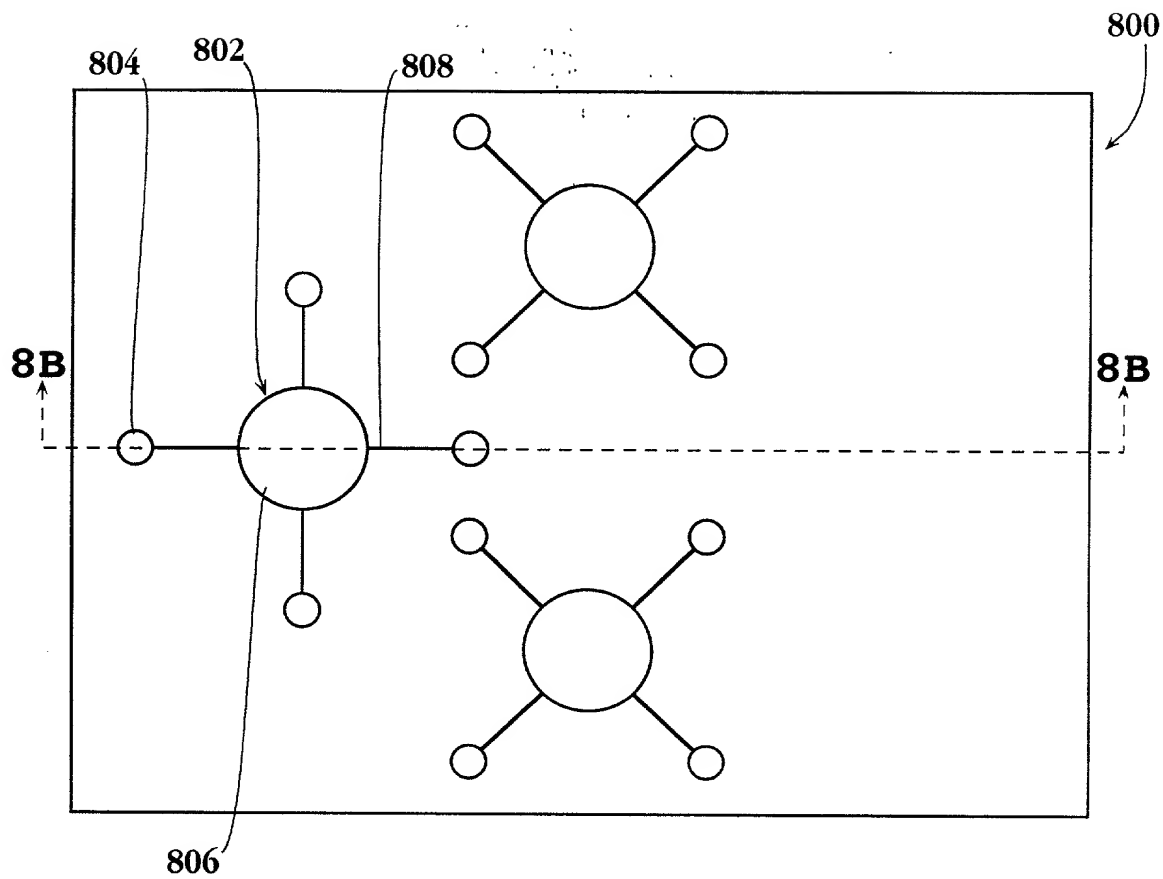
**Fig. 7A**



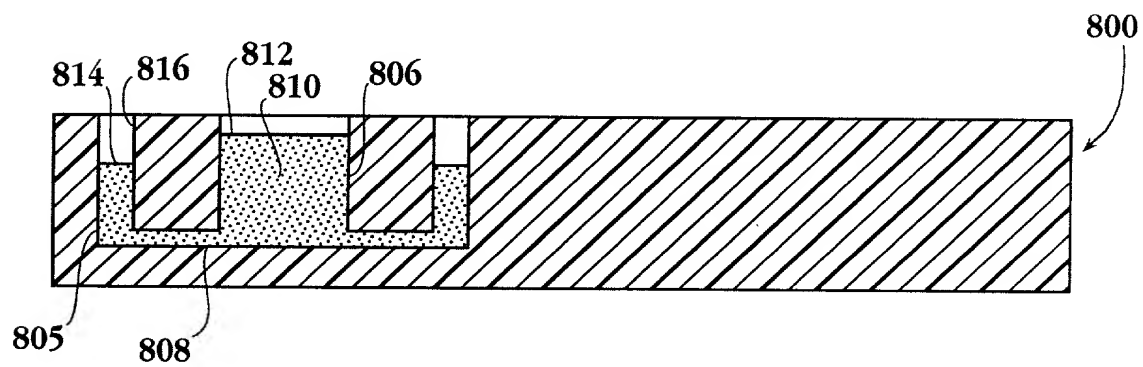
**Fig. 7B**

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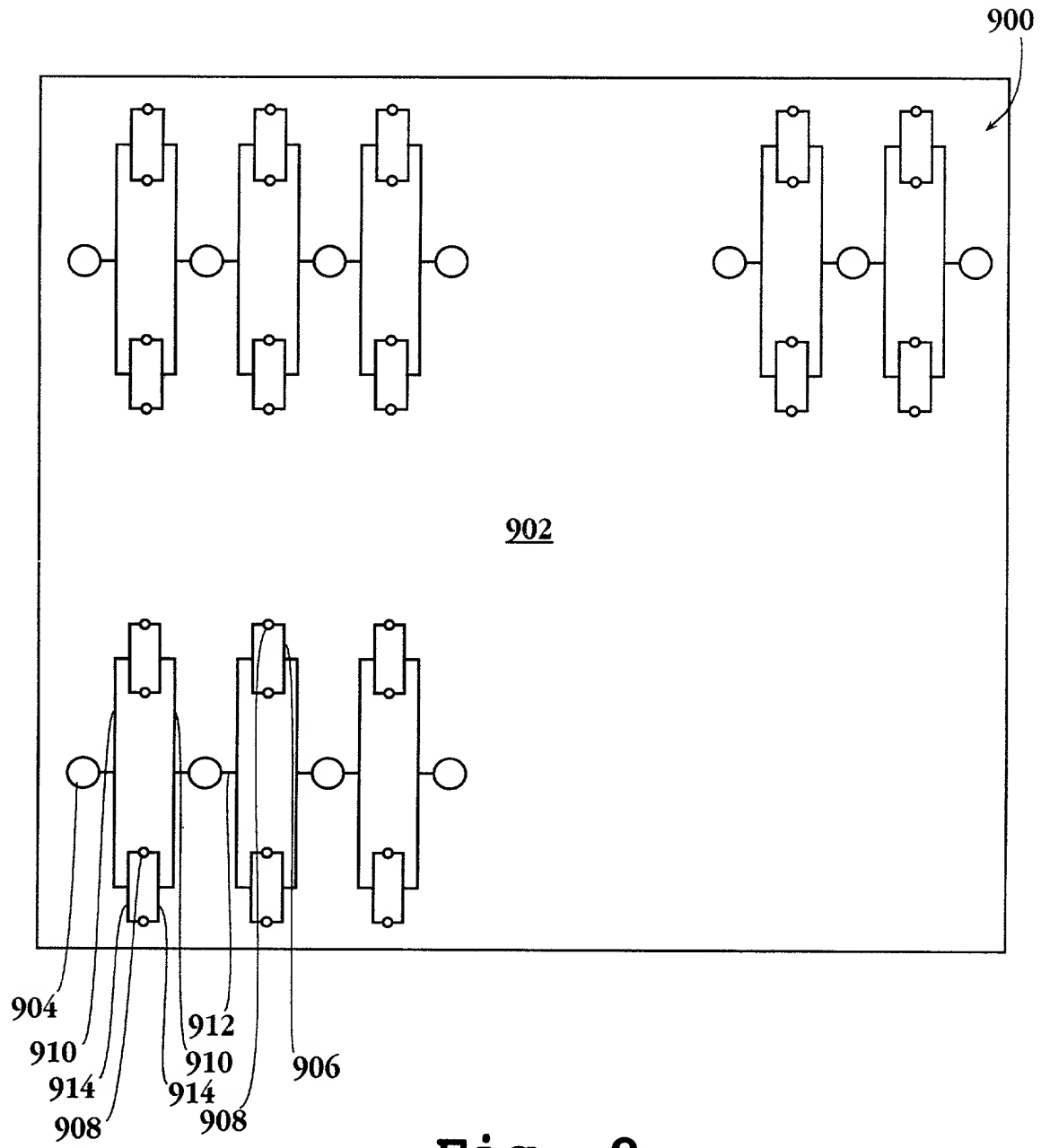




**Fig. 8A**



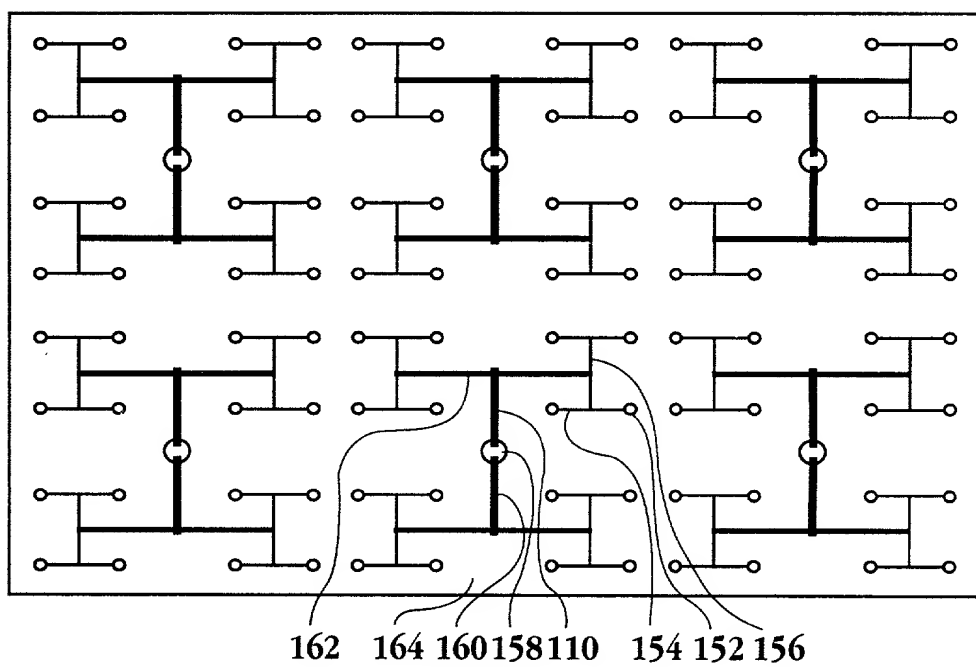
**Fig. 8B**



**Fig. 9**

**Fig. 10**

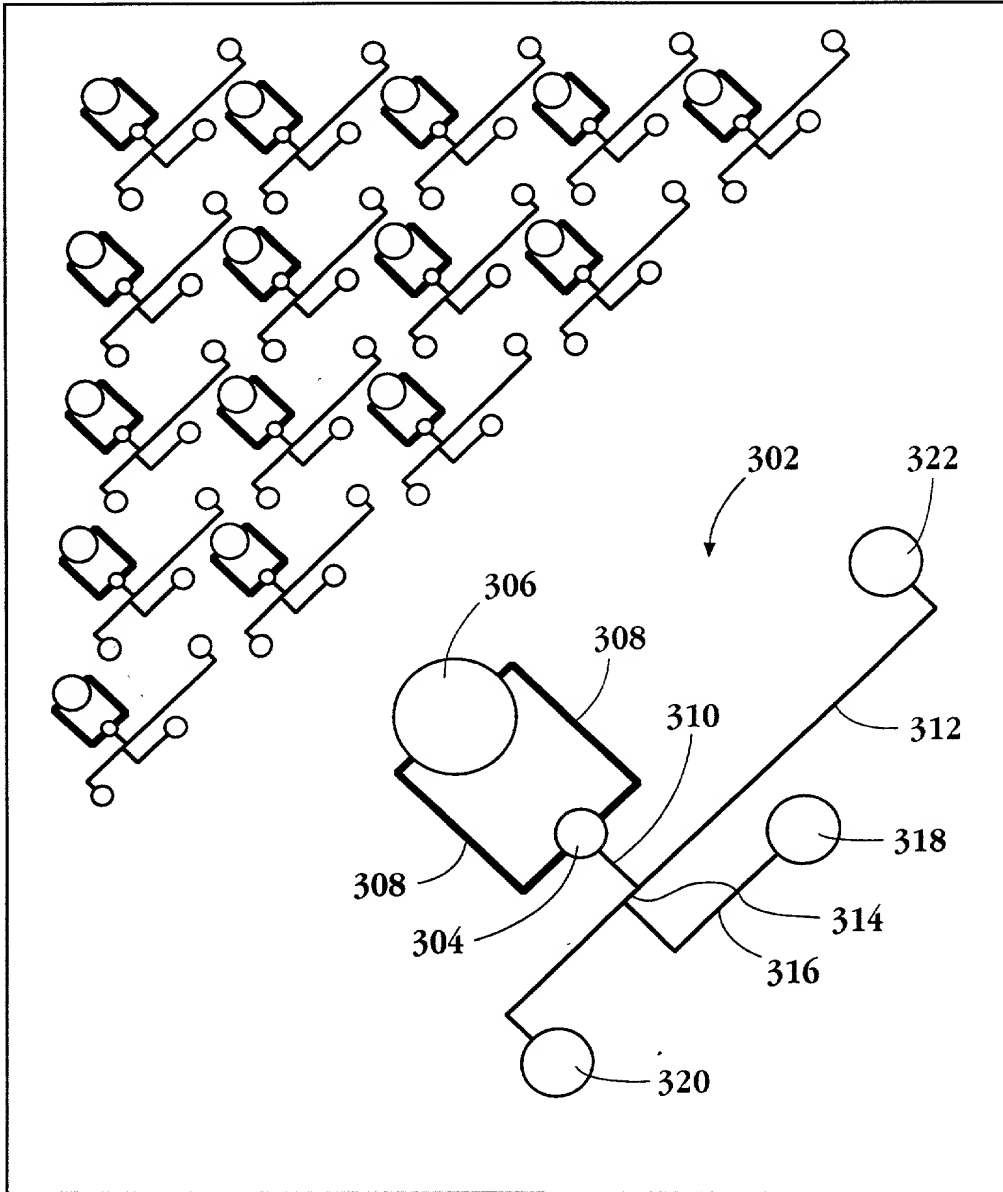
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**Fig. 11**

The diagram illustrates a multi-layer circuit board 200. The top portion shows a perspective view of a grid of conductive traces 202, which are interconnected in a woven pattern. The bottom portion provides a detailed cross-sectional view of a junction 204 where multiple traces meet. This junction is formed by a central conductive core 210, which is surrounded by a dielectric layer 212. The traces 206, 208, 214, and 216 are shown as conductive paths that terminate at the junction. The traces 206 and 208 are connected to a common point 220, while traces 214 and 216 are connected to another common point 222. The entire assembly is supported by a substrate 218, which is shown in cross-section. The top surface of the substrate is labeled 224.

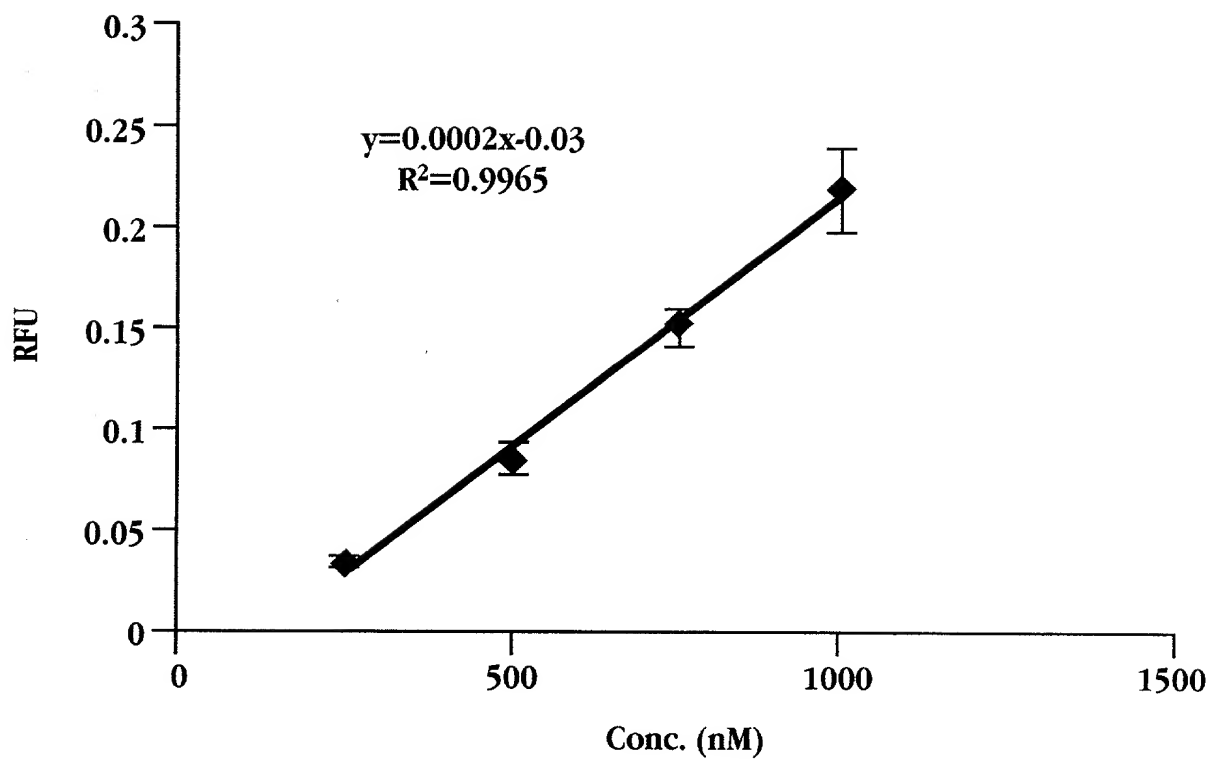
1



**Fig. 13**



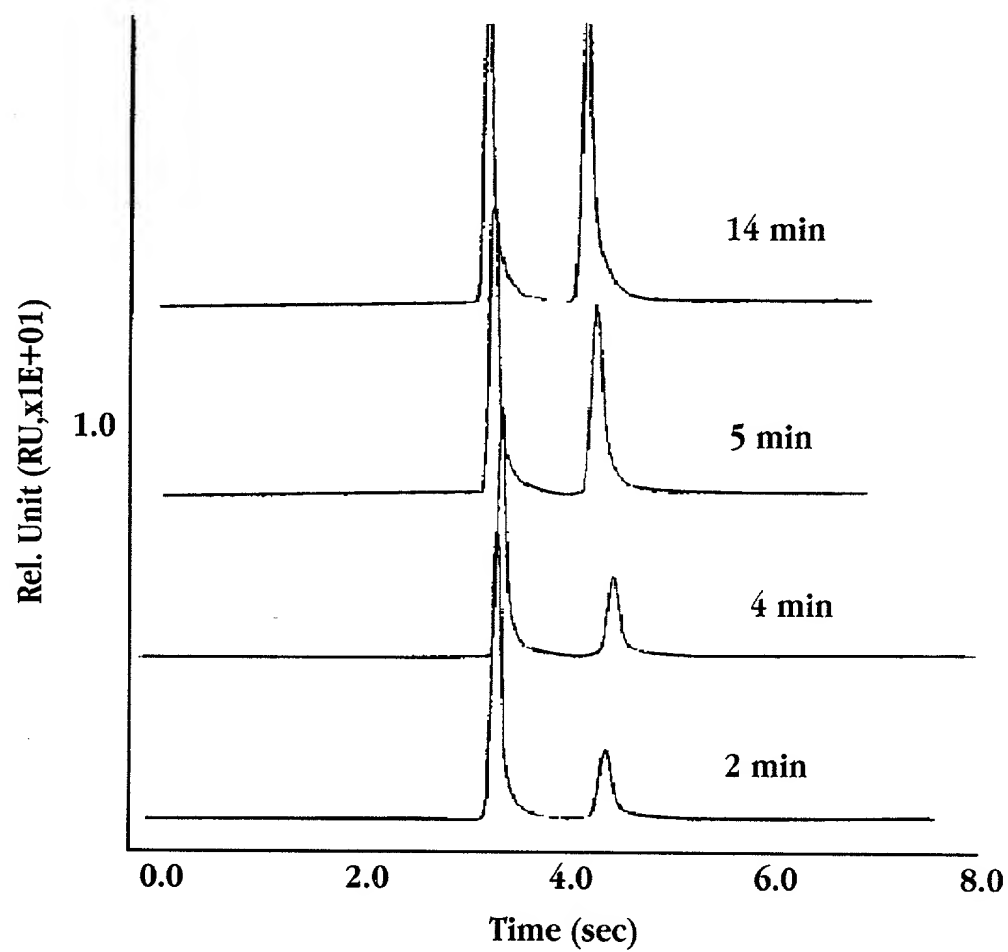
2006-01-01 09:00:00



**Fig. 16**

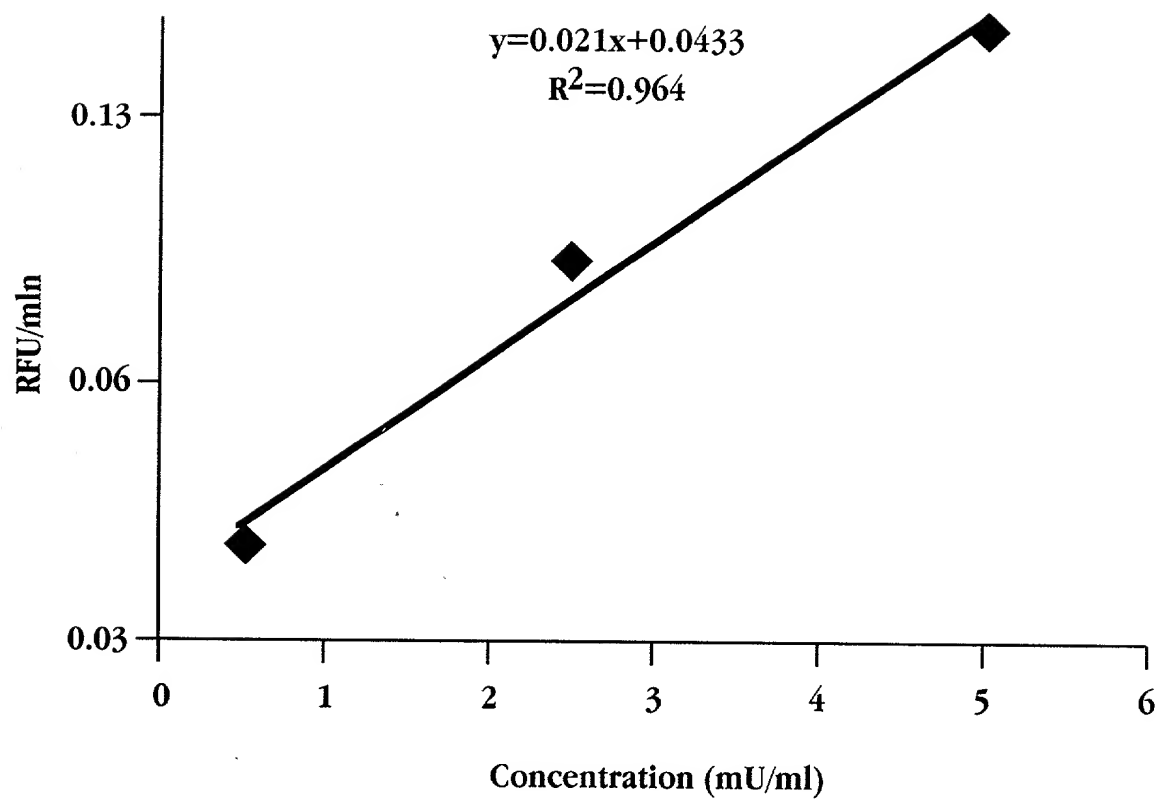


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**Fig. 17**

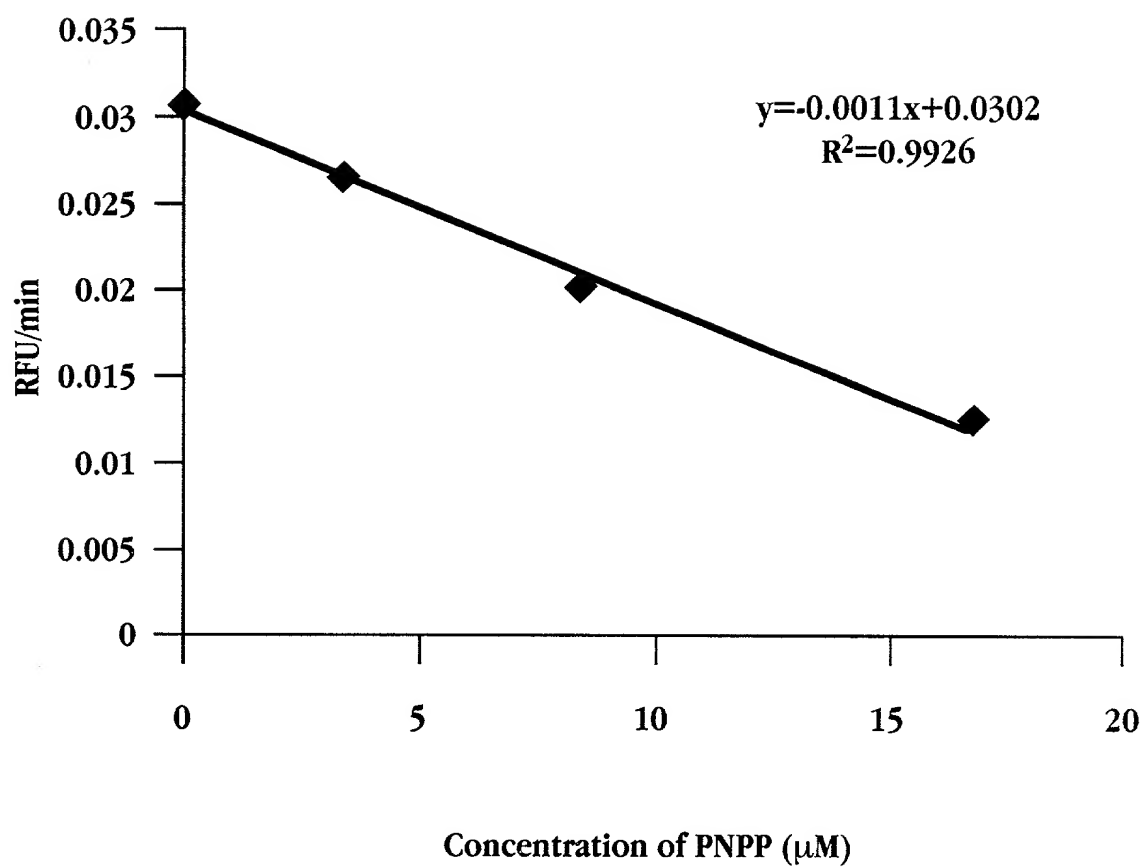
202507-01153600



**Fig. 18**



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**Fig. 20**